行政院國家科學委員會專題研究計畫 成果報告

應用於射頻無線收發器之超低功率奈微機械共振器
研究成果報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 97-2218-E-007-014-
執 行 期 間 ：97 年 11 月 01 日至 99 年 01 月 31 日
執 行 單 位 ：國立清華大學奈米工程與微系統研究所

計 畫 主 持 人：李昇憲

計畫參與人員：此計畫無其他參與人員

處 理 方 式 ：本計畫可公開查詢

中 華 民 國 99 年 03 月 23 日

行政院國家科學委員會補助專題研究計畫成果報告

應用於射頻無線收發器之超低功率奈微機械共振器

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計畫主持人：李昇憲
共同主持人：無
計畫參與人員：陳文健、李銘晃

成果報告類型(依經費核定清單規定繳交)：精簡報告

本成果報告包括以下應繳交之附件：
赴國外出差或研習心得報告一份
出席國際學術會議心得報告及發表之論文各一份

執行單位：國立清華大學奈米工程與微系統研究所

中　華　民　國　九十九　年　一　月　三十一　日

行政院國家科學委員會專題研究計畫成果報告

應用於射頻無線收發器之超低功率奈微機械共振器

Nano/Micro-Mechanical Resonators for Miniaturized Low-Power RF Wireless Transceivers

計 畫 編 號：NSC 97-2218-E-007-014
執 行 期 限：97 年 11 月 01 日至 98 年 10 月 31 日
主　持　人：李昇憲　國立清華大學奈米工程與微系統研究所
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計畫參與人員：陳文健、李銘晃　國立清華大學奈米工程與微系統研究所

一、摘要

本計畫已初步完成 CMOS-MEMS 微機械共振器(Vibrating Micromechanical Resonator)與其整合式轉阻放大器電路之開發，其中共振器本身具備高 *Q* 值、微型體積、低耗能等特性，對於未來開發高性能、低成本之射頻微機械電路，如濾波器、混頻器及振盪器等，已奠定良好的基礎，這類高 *Q* 值電路極可能取代目前無線通訊系統中大量使用的離散式被動元件(Discrete Passives)，以實現單晶片高性能之射頻電路，而成為行動通訊系統的關鍵技術，並可望全面提升台灣在射頻微機電領域的競爭力，期能為台灣開創下一個明星產業。

關鍵詞：CMOS-MEMS、射頻微機電、共振器、高 *Q* 值、無線通訊

Abstract

This project has successfully demonstrated an efficient platform for development of CMOS-MEMS resonators integrated with their associated amplifier circuitry. These high-*Q* resonators are fundamental elements for complicated micromechanical circuits or related sub-systems, such as oscillators, filters, and mixer-filters. To fabricate such CMOS-MEMS resonators, we used CIC/TSMC services to build up the resonator structures followed by a simple release post-process to successfully realize functional CMOS-MEMS resonators with *Q*'s greater than 1,000. Together with on-chip trans-resistance amplifiers, fully integrated CMOS-MEMS resonator circuits were fabricated and have great potential to act as significant building blocks for wireless transceivers. On-chip CMOS-MEMS high *Q* circuits comprised of CMOS-MEMS resonators made by this project, achieving integration, miniaturization, and performance enhancement compared to current technologies, may have huge impacts on future transceiver architectures.

Keywords: CMOS-MEMS, RF MEMS, Resonator, High-*Q*, Wireless Communications

二、緣由與目的

現今的無線通訊架構中，不可避免的要使用許多離散式(Discrete)的機械元件來從事

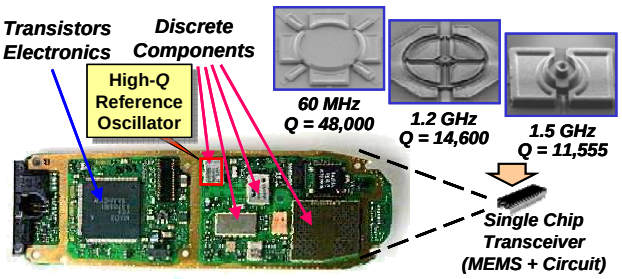

圖 1：手機內部電路板示意圖，其中離散式元件佔有大部分面積，唯有使用射頻微機電技術才能實現單晶片、高度整合的無線射頻收發器。

頻率選擇(Frequency Selection)與頻率產生(Frequency Generation)的重要功能，其原因在於傳統的電子元件(如電感、電容等)無法產生高 Q 值，亦即這些元件在運作時會產生較大的能量損耗；但機械元件藉由低損耗的振動模式可以輕易達到 Q 值超過 10,000 的優異性能，這即是為什麼無線通訊收發系統(如手機)中總是存在需多離散式機械元件，如圖 1 所示，包含表面聲波元件(SAW)、陶瓷元件(Ceramics)或 FBAR (Film Bulk Acoustic Resonator)等，但目前這樣的模式亦造成系統無法積體化(Integration)的困擾，例如這類的機械元件佔據相當大的面積，同時需要介面電路來和電晶體電路進行銜接，其中介面電路所產生的雜散電容會降低系統性能，因此從成本、使用面積、功率消耗與性能的角度來看，均非最佳的解決方案[1] 。

近年來由於射頻微機電(RF-MEMS)技術突飛猛進，我們已經可以製造非常微小的微機械共振器，其 Q 值在數千到數十萬之間[2] [3] ，而射頻微機電技術主要是利用 IC 相容的半導體製程或微機電製程來開發應用於射頻領域的微型元件，包含微機械共振器(Resonator)、振盪器(Oscillator)[4] [5] 、濾波器(Filter)[6] [7] 、混頻器(Mixer)[8] 、微機械開關(Switch)、微型天線(Antenna)、可變電容與電感等元件；對照於傳統的電晶體電路，射頻微機電元件通常具有高 Q 值、低損耗、高阻絕性、高線性度與優異的功率負載能力，但以目前研究進展而言，微機械元件與 IC 電路並無法同時製造，亦即它們必須分屬不同的基材，對於整合(Integration)式系統而言，仍是一大瓶頸。

本計畫將藉由在台灣已初具規模的 CMOS-MEMS 技術，利用現有 CMOS 結構中的材料層，如金屬層或多晶矽層作為機械可動件，因此微機械元件可以自然與電路形成一有效的整合，並搭配簡單 Release 後製程來開發完全整合式的微機械電路，此一 CMOS-MEMS 微機械電路最大的貢獻在於取代傳統 Off-Chip 的石英晶體振盪器或其他高 Q 值離散式元件，使整個無線收發器系統有機會能夠整合在一單晶片電路(Single-Chip Transceivers)上[1] 。

三、研究報告應含的內容

(1) 研究背景

由於使用機械振動原理操作的元件，通常具有高 Q 值的共振特性，例如石英晶體振盪器(Quartz Crystals)或表面聲波元件(Surface Acoustic Wave Devices)等，這類離散式元件的 Q 值通常超過 1,000，是一般純電子元件的數百倍，因此它們早已成為通訊系統中不可或缺的元素；拜日新月異的微機電製造技術所賜，運用共振原理操作的機械元件終於可以縮小到微米(甚至奈米)尺寸，此一微型化工程不但使 CMOS 電路與 MEMS 元件集成化(Integration)的可能性大增(即單晶片的實

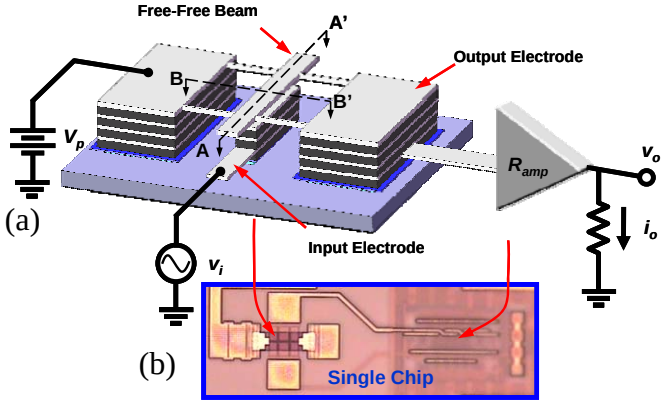

圖 2：(a) CMOS-MEMS 共振器及其放大電路示意圖，包含其量測設置。(b)微機械共振器與電路成功整合的顯微照片。

現)，同時微機械共振器在設計上，更可以覆蓋大部分所需之操作頻率(從數百 kHz 到數個 GHz)，藉以實現無線射頻所需之低損耗頻率選擇(Frequency Selection)與高穩定性頻率產生(Frequency Generation)功能。

(2) CMOS-MEMS 微機械共振器運作與設計

本計畫使用 CIC/TSMC 所提供的 0.35μm 2P4M CMOS 製程，製作 CMOS-MEMS 共振器及其放大電路，如圖 2 所示，這裡僅使用自由樑(Free-Free Beam)共振器為例來說明微機械電路運作方式，但利用此一 CMOS-MEMS 平台可以設計不同幾何形狀、不同材料、不同堆疊方式、不同模態的電容式微機械共振器，我們的目的是希望能夠建立一個單一製程的廣泛共振器平台。

由圖 2(a)可知自由樑共振器是由 CMOS 結構中的第四層金屬(Metal 4)所組成，其材料為鋁，並利用四支細小的支撐樑，銜接於共振器的節點處(Nodal Location)，以提升共振器的 Q 值。電容式共振器的運作原理是在輸入電極施以一 ac 訊號 v_i，並在共振結構上輸入一偏壓 V_P，v_i 與 V_P 的結合會產生靜電驅動力而施加在共振器上，當靜電力的頻率符合共振器結構的共振頻率時，共振器會產生共振模態如圖 3 所示，其結構位移在此一頻率下會被放大 Q 倍；由於共振器結構位移時因電容間隙(Gap)的改變，會形成一時變電容(Time-Varying Capacitance)，若搭配結構偏壓 V_P，最後在電極上會產生輸出的運動電流(Motional Current)，此一電流藉由 On-Chip 的轉阻放大器電路轉換成電壓 v_o 輸出；圖 2(b)顯示 MEMS 共振器與其 CMOS 放大器整合在一起的顯微照片，證明在後製程完成時，微機械結構與電路仍可正常運作。

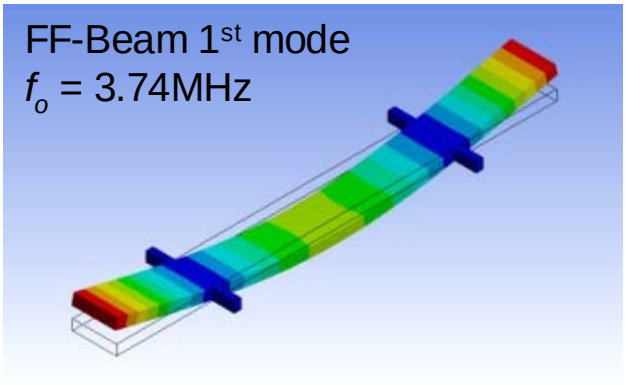

圖 3：CMOS-MEMS 微機械自由樑(Free-Free Beam)共振器第一共振模態。

(3)微機械共振器理論模型的建立

我們以振動學理論為基礎，建立 CMOS-MEMS 微機械共振器的理論模型；這裡以自由樑共振器為例，其共振或操作頻率主要依據方程式(1)來設計，其中 E 為共振器材料 Young's Modulus、ρ為密度、h 為厚度、L_r 為長度。

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k_r}{m_r}} = 1.03\cdot\sqrt{\frac{E}{\rho}}\cdot\frac{h}{L_r^2} \qquad (1)$$

(1)中的等效質量 m_r (Equivalent Mass)、等效彈簧常數 k_r (Equivalent Stiffness)與等效阻尼 c_r (Equivalent Damping Factor)可藉由運動能量理論推導而得[9] ，如方程式(2)所示。

$$m_r(y) = \frac{\rho W_r h\cdot\int_0^{L_r}[X_{mode}(y')]^2(dy')}{[X_{mode}(y)]^2}\ ,$$

$$k_r(y) = \omega_o^2\cdot m_r(y)\ ,$$

$$c_r(y) = \frac{\sqrt{k_r(y)\cdot m_r(y)}}{Q} \qquad (2)$$

其中 X_{mode} 為振動模態、Q 為此機械系統之 Quality Factor。

奈微機械共振器最終需與 CMOS 電路作連結，以完成頻率選擇及頻率產生的功能，因此最理想的處理方式，是將上述機械系統參數 m_r、k_r、c_r 藉由機械與電路領域間的類比關係

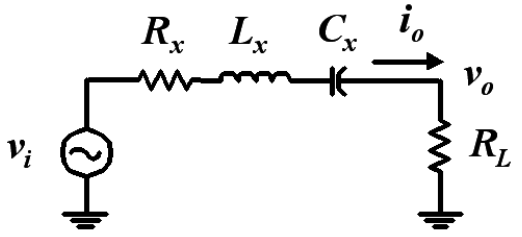

圖 4：CMOS-MEMS 微機械自由樑(Free-Free Beam)共振器之 *RLC* 等效電路。

轉化為電子基本元素 L、C、R。如方程式(3)所示。

$$L_x = \frac{m_r}{\eta_e^2},\ C_x = \frac{\eta_e^2}{k_r},\ R_x = \frac{c_r}{\eta_e^2} \qquad (3)$$

其中為 η_e 為機電轉換係數(Electromechanical Transformer Turns Ratio)，微機械共振器的等效電路如圖 4 所示。最後共振器在共振頻率所產生的輸出運動電流(Motional Current)與運動阻抗(Motional Impedance)為

$$i_o = V_P \cdot \sqrt{\int_{L_{e1}}^{L_{e2}} \int_{L_{e1}}^{L_{e2}} \frac{(\varepsilon_o W_r)^2}{[d(y')d(y)]^2} \frac{k_{re}}{k_r(y')} \frac{X_{mode}(y)}{X_{mode}(y')} dy'\,dy} \cdot \frac{\partial x}{\partial t}$$

$$R_x = \frac{\sqrt{k_r m_r}}{Q\eta^2} \qquad (4)$$

(4)轉阻放大器電路

為了要讀取 CMOS-MEMS 微機械共振器的微小運動電流，微機械共振器必須搭配轉阻放大器電路，將共振器的輸出電流放大而成為電壓輸出。放大器電路上層架構與詳細電路如圖 5 所示。圖 5(b)中的轉阻放大器包含圖左的 Shunt-Shunt Feedback 差動式放大器與圖右的 Common-Mode Feedback 電路；M_1 到 M_5 的 MOS 組成基本的單極差動式放大器，提供主要的放大器阻抗增益；M_{11} 到 M_{18} 組成 Common-Mode Feedback 電路，用以設定輸出

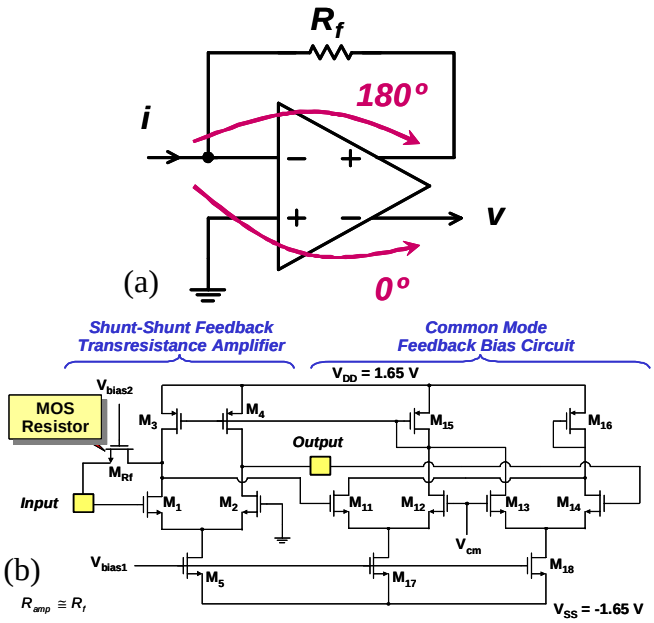

圖 5：CMOS 轉阻放大器(a)電路上層架構、(b)電晶體電路詳圖。

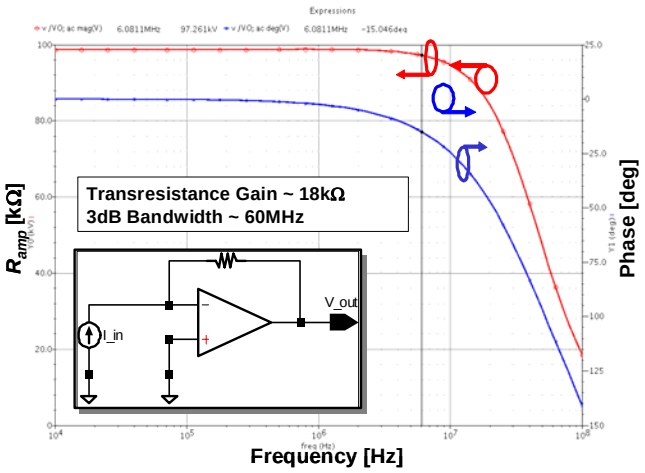

圖 6：CMOS 轉阻放大器(a)電路上層架構、(b)電晶體電路詳圖。

端的直流偏壓位準；M_{Rf} 為 MOS 電阻，提供放大器主要的阻抗增益，可藉由改變其閘極電壓，調整放大器阻值增益與頻寬。利用單級放大器(對照多級放大器)的好處在於操作的頻寬較大與產生的雜訊較小，同時因為電晶體的使用數量較少，自然消耗的功率也較低。

圖 6 顯示轉阻放大器的模擬結果(Post-Simulation)，其阻抗增益為 18kΩ，頻寬為 60MHz，對於共振頻率在數 MHz 的 CMOS-MEMS 共振器而言已綽綽有餘。

(5) CMOS-MEMS 製程

此計畫使用 TSMC 0.35μm 2-Poly 4-Metal CMOS 製程，共振結構可選擇使用鋁金屬、

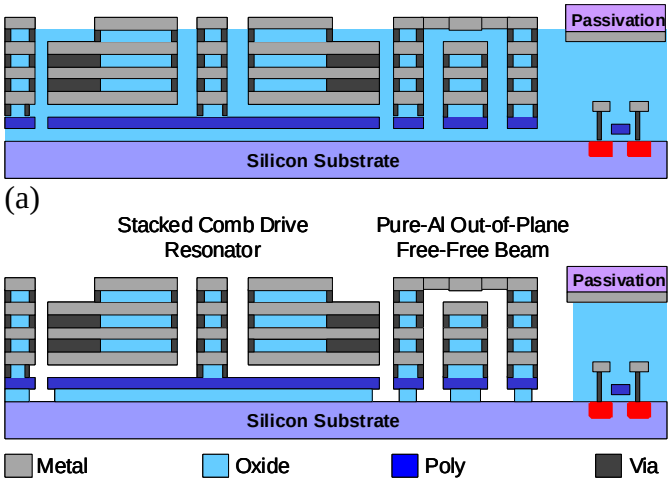

圖 7：CMOS-MEMS 共振器與電路製造流程。(a) Release 前；(b) Release 後。

多晶矽、氧化矽或以上材料的組合，以期找出最佳化的共振器架構。我們選擇 Cadence 為主要佈局軟體，以強化未來 MEMS 元件與 CMOS 電路的整合佈局與模擬。

圖 7 說明本計畫 CMOS-MEMS 製程平台的製造流程，圖 7(a)為由 CMOS Foundry 廠取得之晶片，其中 MEMS 區域的保護層(Passivation Layer)已經去除，而 CMOS 電路上的保護層仍然保留；經由簡單的等向性濕式蝕刻(使用商用的 SiO_2 蝕刻液)，MEMS 區域的 SiO_2 會被去除而留下金屬或被金屬包覆的可動件，如圖 7(b)所示，CMOS 電路部分因保護層的阻隔，因此不受影響。值得一提的是這樣的後製程並不需要額外的光罩，為 Maskless Process，另外在元件釋放的過程中，並不需要使用 Super Critical Point Dryer，因此極為簡單、便宜。

圖 7 製程示意圖亦顯示堆疊式的 Comb-Drive 共振器(具有鋁、SiO_2、鎢等材料來作為共振器結構)與純鋁自由樑共振器可以同時藉由此一 CMOS-MEMS 製程平台實現，因此我們認為此平台可適用於不同幾何外型、不同材料組合、不同模態的共振器，可視為一共振器之通用製程，非常適合學術界或 Design House 之類的公司進行快速的研發工作。圖 8 顯示純鋁的自由樑共振器與複合結構的 Comb-Drive 共振器顯微照片，其中圖 8(b)為自由樑支撐結構放大圖，在此可以明顯看出其支撐位置設計在共振器的運動節點處(Nodal Locations)，如圖 3 所示，以減少能量損耗而達到高 Q 值；圖 8(d)為 Comb-Drive 共振器的梳齒電極放大圖，可以清楚看到結構是由不同材料疊層組成。

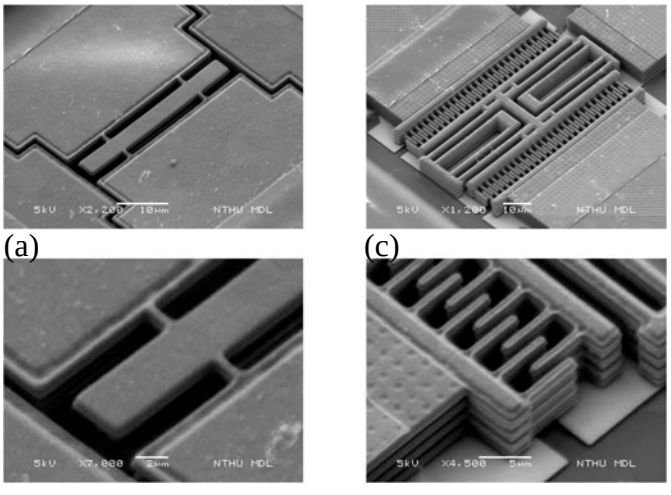

圖 8：CMOS-MEMS 共振器 SEM 照片。(a)自由樑全景；(b)自由樑節點支撐放大圖；(c) Comb-Drive 共振器全景；(d) Comb-Drive 共振器梳齒部分放大圖。

(6) 量測結果

由於本計畫設計的共振器以低頻撓曲模態(Flexural Mode)為主，易受到空氣阻尼(Air Damping or Squeezed Film Damping)影響而降低共振器的 Q 值，同時其運動阻抗(Motional Impedance)亦大幅增加，如方程式(4)所示，因此我們必須在真空中量測，以實現共振器的最佳性能。

我們將 CMOS-MEMS 共振器(已含轉阻放大器電路)置於陶瓷基材(Ceramics)上，並透過打線(Wire Bonding)與電路板進行電路連

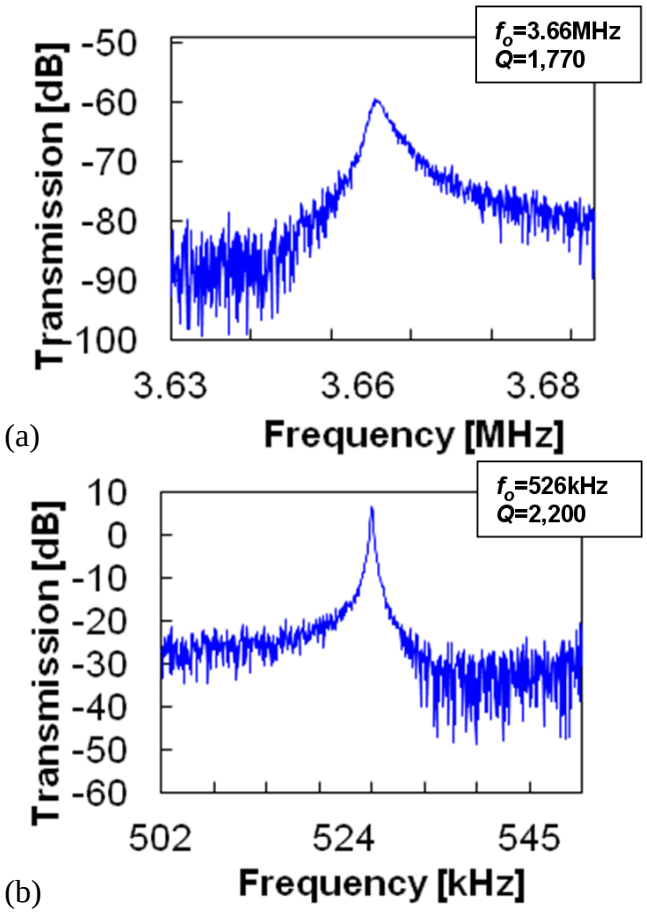

圖 9：CMOS-MEMS 共振器之量測頻譜特性。(a)自由樑共振器；(b) Comb-Drive 共振器。

接；電路板最終會放置於我們特殊設計的玻璃腔體內，藉由真空幫浦(Vacuum Pump)將腔體內的壓力抽至 200μTorr 後始進行量測。圖 9 顯示 CMOS-MEMS 共振器在真空中的量測結果，其中圖 9(a)為長 40μm 的自由樑共振器與其所屬電路之頻譜特性，共振器結構之材料為鋁，共振頻率在 3.66MHz，與圖 3 之有限元素分析結果相當吻合，頻率誤差為 2.2%，誤差主要來自於楊式係數的估計誤差(Foundry 廠並沒有提供精確的楊式係數)；自由樑共振器的 *Q* 值為 1,770，對照於一般 *Q* 值僅數百的固定樑(Clamped-Clamped Beam)共振器而言，節點支撐(如圖 8(b)所示)阻絕了大部分的能量損耗，因此對於自由樑共振器 *Q* 值的提升有極大的助益。圖 9(b)為 Comb-Drive 共振器與其放大器電路的頻譜量測特性，此共振器的材料結構使用複合堆疊的方式，堆疊材料包含鋁、鎢與 SiO_2，共振頻率在 526kHz，*Q* 值為 2,200。

(7) 結論

本計畫使用 CMOS Foundry 既有的電晶體電路製程，加上簡易的濕式蝕刻後製程(不需額外的光罩)，開發出一通用的射頻微機械共振器/電路平台，透過此一製程平台，我們可以有效將微機電(MEMS)元件與電路(CMOS)整合在單一晶片上；此外，藉由 CMOS 電路多樣的材料堆疊特性，此平台共振器結構的材料選擇亦非常多元，並可以變化出不同組合，本計畫設計兩種不同的共振器可清楚的說明這一個優勢。

CMOS-MEMS 共振器與相關整合式電路的研究開發，不僅能夠全面性提升台灣在射頻微機電(RF MEMS)領域的設計、製造與量測能力，更可能為台灣開創下一個明星產業，如時基元件(Timing Reference Components)與濾波(Filtering)等無線通訊亟需的功能。

四、參考文獻

[1] C. T.-C. Nguyen, “Vibrating RF MEMS for next generation wireless applications (invited),” *Proceedings*, 2004 IEEE Custom Integrated Circuits Conf., Orlando, Florida, Oct. 3-6, 2004, pp. 257-264.

[2] J. Wang, Z. Ren, and C. T.-C. Nguyen, “1.156-GHz self-aligned vibrating micromechanical disk resonator,” *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 51, no. 12, pp. 1607-1628, Dec. 2004.

[3] S.-S. Li, Y.-W. Lin, Y. Xie, Z. Ren, and C. T.-C. Nguyen, “Micromechanical “hollow-disk” ring resonators,” *Technical Digest*, IEEE Int. Conf. on Micro Electro Mechanical Systems, Maastricht, The Nether-lands, 2004, pp. 821-824.

[4] Y.-W. Lin, S. Lee, S.-S. Li, Y. Xie, Z. Ren, and C. T.-C. Nguyen, “Series-resonant VHF micromechanical resonator reference oscillators,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2477-2491, Dec. 2004.

[5] Y.-W. Lin, S.-S. Li, Z. Ren, and Clark T.-C. Nguyen, “Low phase noise array-composite micromechanical wine-glass disk oscillator,” *Technical Digest*, 2005 IEEE International Electron Devices Meeting, Washington, DC, Dec. 5-7, 2005, pp. 287-290.

[6] K. Wang and C. T.-C. Nguyen, “High-order medium frequency micromechanical electronic filters,” *IEEE/ASME J. Microelectromech. Syst.*, vol. 8, no. 4, pp. 534-557, Dec. 1999.

[7] F. D. Bannon III, J. R. Clark, and C. T.-C. Nguyen, “High-*Q* HF micro-electromechanical filters,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 4, pp. 512-526, April 2000.

[8] A.-C. Wong and C. T.-C. Nguyen, “Micromechanical mixer-filters (“mixlers”),” *IEEE/ASME J. Microelectromech. Syst.*, vol. 13, no. 1, pp. 100-112, Feb. 2004.

[9] K. Wang, A.-C. Wong, and C. T.-C. Nguyen, “VHF free-free beam high-Q micromechanical resonators,” *IEEE/ASME J. Microelectromech. Syst.*, vol. 9, no. 3, pp. 347-360, Sept. 2000.

計畫成果自評

本計畫原先預定使用計畫主持人於美國密西根大學所開發之微機電製程，以實現計畫所需之微機械共振器，但由於台灣在半導體產業的優勢及政府挹注於國家晶片中心的豐沛資源使得我們決定將研究重心轉向利用 CMOS-MEMS 來實現無線通訊所需之高 *Q* 值微機械電路，結果證明我們選擇的道路是正確的，目前成果已遠遠超出原先計畫目標，成功開發出低成本、高量率之 CMOS-MEMS 共振器通用製程平台，可提供不同類型的共振器與 IC 電路整合的環境，未來也將提供頻率控制與無線通訊產業所需的關鍵元件或系統，發展潛力可期。

附件一：論文發表

國際研討會	論文名稱
2010 IEEE MEMS Conference	A Generalized Foundry CMOS Platform For Capacitively-Transduced Resonators Monolithically Integrated With Amplifiers
2010 IEEE MEMS Conference	Realizing Deep-Submicron Gap Spacing For CMOS-MEMS Resonators With Frequency Tuning Capability Via Modulated Boundary Conditions

附件二：赴國外出差或研習心得報告一份

附件三：出席國際學術會議心得報告

A GENERALIZED FOUNDRY CMOS PLATFORM FOR CAPACITIVELY-TRANSDUCED RESONATORS MONOLITHICALLY INTEGRATED WITH AMPLIFIERS

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ABSTRACT

A generalized foundry CMOS-MEMS platform suited for integrated micromechanical resonator circuits have been developed for commercial multi-user purpose and demonstrated with a fast turnaround time and a variety of design flexibilities for resonator applications. With this platform, different configurations of capacitively-transduced resonators monolithically integrated with their associated amplifier circuits, spanning frequencies from 500kHz to 14.5MHz, have been realized with resonator *Q*'s around 2,000. This platform specifically featured with various configurations of structural materials, different arrangements of mechanical boundary conditions, large transduction area, well-defined anchors, and performance enhancement scaling with IC fabrication technology, offers a variety of flexible design options suited for sensor and RF applications.

INTRODUCTION

The present wireless transceivers composed of conventional off-chip mechanical resonators and filters limit the miniaturization of communication devices as well as impede the cost-down and system integration for portable electronics. In order to reduce size, power consumption, and increase *Q*, vibrating micromechanical circuits fabricated using IC-compatible MEMS technologies have been developed towards the integration with on-chip RF transistor circuits [1]. However, prior approaches for CMOS-MEMS integration, such as mixed process [2][3], MEMS-first [4][5], and MEMS-last [6][7] strategies, requires enormous complexity and compromise of fabrication processes, impeding the fast cycling time of nowadays product development and of course causing huge barrier for industrial design houses. As a solution to aforementioned issues, foundry CMOS-MEMS platform such as dry-release-based [8] and wet-release-based [9] approaches provides ease of use, fast prototyping, and circuit integrated characteristics for vibrating RF-MEMS applications. Nonetheless, [8] confronts high motional impedance of their fabricated

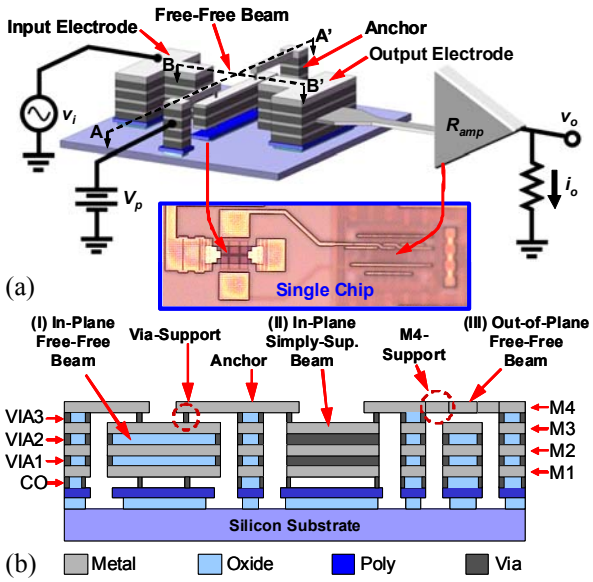

Fig. 1: Perspective-view schematic of (a) a CMOS-MEMS free-free beam resonator monolithically integrated with amplifier circuits. (b) Cross-section view (A-A') of resonators fabricated using the proposed platform.

resonators due to the relatively large electro-to-resonator gap spacing from RIE-etched constraint while both [8] and [9] suffer the deficiency in design flexibilities on structural material configurations, mechanical boundary conditions, vibrating modes, multi-dimensional motions, and well-defined anchor geometry without affection of release undercut.

To overcome the abovementioned deficiency, this work develops a generalized platform utilizing TSMC 0.35μm 2-Poly-4-Metal process with a simple maskless release process, demonstrating ease of use, low cost, fast turnaround time, and innate MEMS-circuit integration. Various configurations of capacitively-transduced CMOS-MEMS resonators monolithically integrated with circuits have been demonstrated using this platform with resonance frequencies spanning from 0.5MHz to 14.5MHz and with *Q*'s up to 2,200. In addition, the major bottleneck of capacitive resonators due to high motional impedance R_x is alleviated when the electrode-to-resonator

gap spacing, of which R_x is proportional to the 4th power, can be scaled down with advanced IC technology, e.g., 0.18μm or even smaller feature-size CMOS process.

PLATFORM & DEVICE OPERATION

To demonstrate most of the new features used in this platform, a laterally vibrating free-free beam resonator [10] with via-supported scheme, as shown in Fig. 1, is exemplified here to present that a composite resonator structure is formed utilizing metal (i.e., aluminum and tungsten) and SiO_2 while supported by vias (VIA) and contacts (CO) which serve not only electrical interconnects but mechanical supports to effectively conserve vibrating energy within resonator bodies due to the tiny size of these supports. As shown in Fig. 1(a), an on-chip trans-impedance amplifier is also integrated with resonators to resolve (1) parasitic feedthroughs from bond pads and (2) impedance mismatches between resonators and the 50Ω-based testing facilities, allowing us to directly measure the motional current induced by vibrating motions of resonators without the masking effects from feedthrough parasitics. To maximize the electro-mechanical coupling, the minimum electrode-to-resonator gap spacing of 0.5μm in this foundry process is formed between two smooth sidewalls of metal/via composite where the transduction areas are greatly improved, allowing smaller motional impedance for the resonators.

As shown in Fig. 1(b), CMOS-MEMS resonators fabricated using the proposed platform specifically possess several unique features including (1) complex structural materials which can be made of metal/oxide composite (case I), metal composite (case II), and pure metal (case III); (2) various mechanical boundary conditions of resonators such as fixed (not shown here), simply-supported (case II), and free end (case I & III) designs; (3) multi-dimensional displacements of resonators capable of in-plane (case I & II) and out-of-plane (case III) motions to the substrate surface; (4) standard CMOS vias (VIA) and contacts (CO) acting as tiny supports of resonators (case I & II), to effectively isolate the vibrating energy from resonators to their anchors, (5) well-defined anchors without undercut issue which is often seen in conventional CMOS-MEMS or SOI process; (6) better transducer

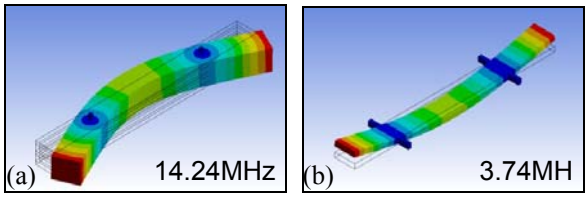

Fig. 2: Finite element simulated mode shapes for CMOS-MEMS free-free beam resonators. (a) In-plane mode. (b) Out-of-plane mode.

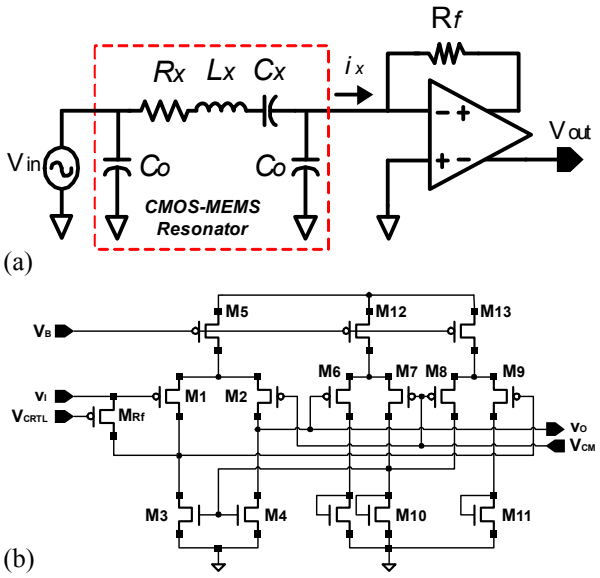

Fig. 3: (a) Top-level circuit schematic and (b) detail circuit schematic of the single-stage trans-impedance amplifier used in this work.

efficiency attained by utilizing via-connected walls (case I & II) to form a flat sidewall electrodes, all of which offer a variety of flexible options suited for sensor and RF applications.

To excite this device (shown in Fig. 1(a)), an ac signal v_i together with a dc-bias voltage V_P would generate an electrostatic force driving the beam into the corresponding vibration mode shape shown in Fig. 2(a) while Fig. 2(b) presents vibrating motion of case III in Fig. 1(b) for comparison. This motion creates time-varying capacitance between the beam and output electrode, sourcing out an output current i_o which would enter an on-site amplifier with a designed impedance gain. Fig. 3(a) presents the top-level schematic of the trans-impedance amplifier circuit used in this work to transfer the input motional current of vibrating resonators into voltage output with certain amplification factor R_f. In the detailed circuit schematic of Fig. 3(b), transistors M_1-M_5 comprise the basic single stage, differential op amp while M_6-M_{13} constitute a common-mode feedback circuit that sets its output dc bias point. The MOS resistor M_{Rf} provides resistance R_f and serves as shunt-shunt feedback element that allows control of the trans-impedance gain via adjustment of its gate voltage.

FABRICATION

To fabricate resonators using the presented platform, chips were manufactured utilizing standard 0.35μm 2-Poly-4-Metal CMOS service from TSMC with a cross-section view shown in Fig. 4(a). Then a commercial SiO_2 etchant with very high selectivity to metal layers, vias, and contacts is utilized to release

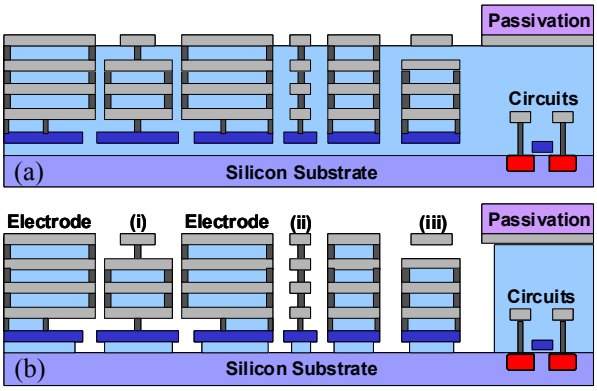

Fig. 4: Cross-sections depicting the fabrication process used to achieve CMOS-MEMS resonators. (a) After standard CMOS process. (b) After wet release process. Various types of resonators are realized using this platform, including (i) via-supported free-free beam (B-B' of Fig. 1(a)), (ii) simply-supported beam, and (iii) pure-metal free-free beam.

the resonator structures depicted in Fig. 4(b) without the helps of critical point dryers while the transistor circuits is protected by the passivation layer of silicon nitride. Please note that the via-connected sidewalls not only increase the transduction areas but also protect the inner SiO_2 without attacks by the release etchant, providing metal/oxide composite which might benefits temperature compensation scheme for future timing reference devices.

Fig. 5 presents the SEM's of fabricated CMOS-MEMS resonators, including (a) a chip global view, (b) a via-supported in-plane free-free beam, (c) a pure-metal out-of-plane free-free beam, (d) an in-plane simply-supported beam, and (e) an in-plane clamped-clamped beam, showing that this platform is capable of producing resonators with various modes, different mechanical boundary conditions, in-plane and out-of-plane directions of motions, and diversified supporting structures. During the wet release process of Fig. 5(b), via/contact supports of Fig. 6 are clearly seen, providing enough mechanical strength to support resonator body even when dc-bias voltage of more than 100V is applied. Please note that the anchored plane in Fig. 6(d) is still intact, offering a rigid anchor structures without affection of undercut issue often seen in other fabrication technologies.

EXPERIMENTAL RESULTS

The fabricated resonators with their amplifier circuits in Fig. 5 were tested under controlled pressure of 20μTorr using a custom-built chamber with an electrical hook-up of Fig. 7 for a conventional two-port measurement. The RF-Out port of an HP 8753ES network analyzer is connected directly to metal electrode of the CMOS-MEMS resonators inside the vacuum chamber while the analyzer's RF-In port is

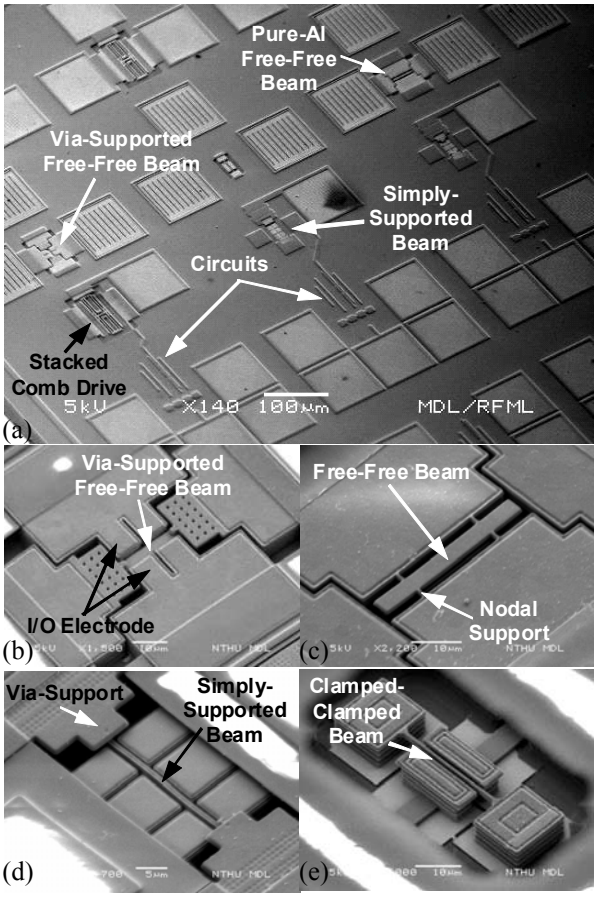

Fig. 5: The SEM views of fabricated CMOS-MEMS resonators. (a) Overall-view of a chip. (b) Via-supported in-plane free-free beam. (c) Pure-metal out-of-plane free-free beam. (d) In-plane simply-supported beam. (e) Clamped-clamped beam.

connected to the output electrodes of CMOS amplifier circuitry. The dc bias voltage is connected to the body of the resonator.

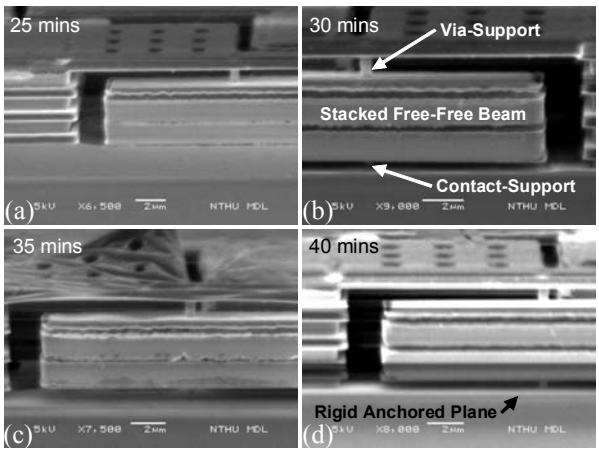

Fig. 6: The SEM views of wet release process for CMOS-MEMS resonators with (a) 25-min, (b) 30-min, (c) 35-min, and (d) 40-min release time.

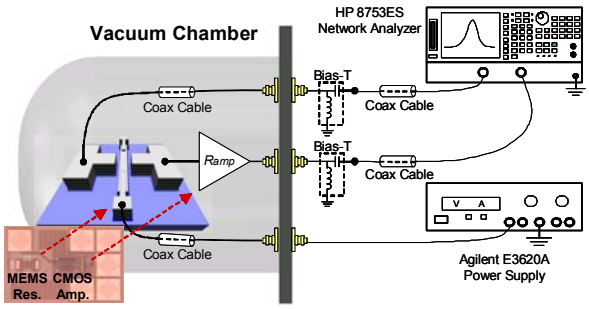

Fig. 7: Schematic illustrating the measurement scheme showing detailed connections for measurement instrumentation.

Fig. 8 presents the measured spectra for the CMOS-MEMS resonators with their integrated amplifiers spanning frequencies from 0.5MHz to 14.5MHz with *Q*'s in a range of 800 to 2,200, verifying the efficacy of this platform. Furthermore, Fig. 9 shows the measured frequency characteristics for a stacked comb-drive resonator in Fig. 5(a) under different measurement conditions. The transmission spectrum of the resonator integrated with its amplifier under vacuum obviously outperforms the measured results of other conditions such as resonators tested with amplifier circuit in air (red spectrum) and devices tested without circuit under vacuum (green spectrum), indicating integration of MEMS and circuits is crucial for device performance enhancement.

CONCLUSIONS

This work presents a general and easy-to-use platform provided for users to facilitate design and development of high-*Q* MEMS resonating devices integrated

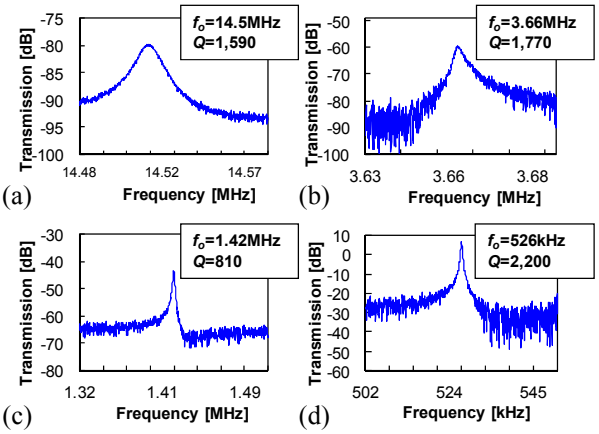

Fig. 8: Measured frequency characteristics in vacuum for fabricated CMOS-MEMS resonators. (a) Via-supported in-plane free-free beam of Fig. 5(b). (b) Out-of-plane free-free beam of Fig. 5(c). (c) In-plane simply-supported beam of Fig. 5(d). (d) Stacked comb-drive resonator of Fig. 5(a).

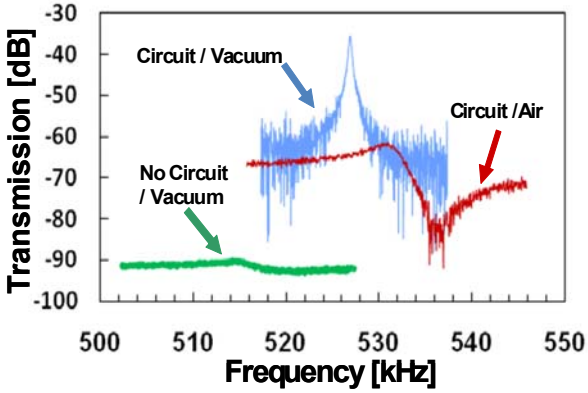

Fig. 9: Measured frequency characteristics for stacked comb-drive resonators of Fig. 5(a) under different measured conditions, including vacuum with amplifier, air with amplifier, and vacuum without amplifier.

with circuits, capable of achieving single-chip implementation for sensors and communication applications. In addition, fully-integrated CMOS-MEMS resonator circuits, occupying die area of only 340μm x 110μm in this work, offers very small form factor and low power consumption suited for future portable applications.

ACKNOWLEDGMENT

This work was supported by the National Science Council (NSC) of Taiwan under grant of NSC -97-2218-E-007-014. The authors also wish to appreciate the TSMC and National Chip Implementation Center (CIC), Taiwan, for supporting the IC Manufacturing.

REFERENCES

[1] C. T.-C. Nguyen, *Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 54, no. 2, pp. 251-270, 2007.
[2] T. Core, *et al.*, *Tech. Digest, Solid State Technology*, pp. 39-44, 1993.
[3] C. T.-C. Nguyen, *et al.*, *J. Solid-State Circuits*, vol. 34, no. 4, pp. 440-455, April 1999.
[4] J. H. Smith, *et al.*, *Tech. Digest, IEDM'95*, pp. 609-612, 1995.
[5] A. B. Graham, *et al.*, *Tech. Digest, MEMS'09*, Sorrento, Italy, pp. 23-26, 2009.
[6] W.-L. Huang, *et al.*, *Tech. Digest, MEMS'08*, Tucson, Arizona, pp. 10-13, 2008.
[7] J. Costa, *et al.*, *Tech. Digest, Hilton Head'08*, Hilton Head Island, South Carolina, pp. 18-21, 2008.
[8] C. Lo, *et al.*, *Tech. Digest, Transducers'05*, Seoul, Korea, pp. 2074-2077, 2005.
[9] J. Teva, *et al.*, *Tech. Digest, MEMS'08*, Tucson, Arizona, USA, pp. 82-85, 2008.
[10] K. Wang, *et al.*, *J. Microelectromech. Syst.*, vol. 9, no. 3, pp. 347-360, Sept. 2000.

REALIZING DEEP-SUBMICRON GAP SPACING FOR CMOS-MEMS RESONATORS WITH FREQUENCY TUNING CAPABILITY VIA MODULATED BOUNDARY CONDITIONS

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ABSTRACT

Integrated CMOS-MEMS array resonators have been demonstrated that takes advantage of pull-in effect to surmount limitations of CMOS foundry process and attains electrode-to-resonator gap spacing at a deep-submicron range, leading to much smaller motional impedance compared to conventional CMOS-MEMS technologies, while possessing unique frequency tuning capability by modulating their mechanical boundary conditions. With the increase of applied dc-bias which simultaneously serves for functions of pull-in and resonator operation, the upward frequency shift of resonance caused by boundary condition ("BC") change offers opposite tuning mechanism to well-known effect of electrical stiffness. As a result, frequency variation induced by BC-modulation and electrical-stiffness would yield a frequency-insensitive region under a certain dc-bias.

INTRODUCTION

Off-chip vibrating mechanical devices such as SAW and quartz crystals are widely used in wireless transceivers as front-end filters and timing reference devices. However, their bulky size and discrete nature impede the integration and performance enhancement for future multi-mode wireless systems which require considerable quantities of high-Q resonators. To replace these discrete mechanical devices, on-chip micromechanical resonators have been developed in the past ten years with frequencies from tens of kHz to a few GHz and with sufficient Q's, hence paving a way of miniaturizing and integration for future wireless communications [1][2]. However, these technologies still suffer process complexity, performance comprise, and cost increase for achieving resonators monolithically integrated with circuitry [3][4].

As efficacious solutions to realizing integration of micromechanical resonators and their associated circuits, CMOS-MEMS technologies offer a simple and low cost approach using CMOS foundry service together with maskless release process, now successfully demonstrating on-chip high-Q micromechanical

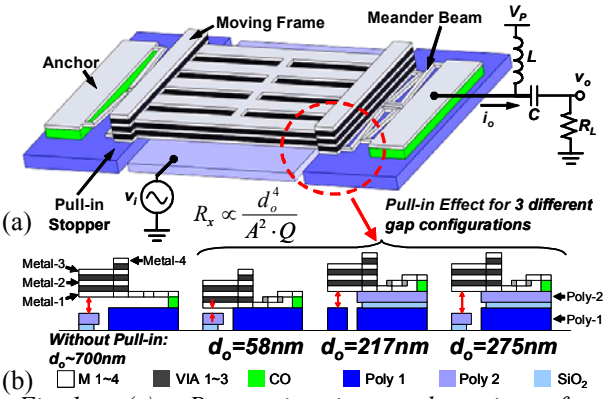

Fig. 1: (a) Perspective-view schematic of a CMOS-MEMS beam-array resonator in a typical one-port bias and excitation setup. (b) Original electrode-to-resonator gap spacing and three different gap configurations after pull-in.

resonators integrated with CMOS circuitry [5][6][7]. However, all of abovementioned CMOS-MEMS technologies confront the limitation of minimum feature sizes of CMOS technology, hence causing high motional impedance due to the relatively large electrode-to-resonator gap spacing of the fabricated resonators. Although such gaps can be scaled down with advanced CMOS process (e.g., 90nm or smaller), the cost in MEMS devices would tremendously increase with over qualification of related CMOS circuitry.

This work introduces an effective approach in standard CMOS-MEMS technology to greatly reduce the electrode-to-resonator gap spacing without the need of advanced CMOS process, hence providing a cost-effective solution to alleviate performance degradation of resonators using conventional CMOS-MEMS techniques. With the well-known electrostatic pull-in effect, three different gap-reduction configurations utilizing the existing layers of 0.35μm 2-poly-4-metal CMOS technology have been demonstrated to achieve deep-submicron gaps, significantly lower the motional impedance of the fabricated CMOS-MEMS resonators. Using gap reduction mechanism depicted in Fig. 1, beam-array resonators centered in HF range with gaps of 58nm, 217nm, and 275nm, respectively, have been demonstrated that achieves comparable electro-mechanical coupling with their non-CMOS-MEMS counterparts [1]. In addition, mechanical boundary condition

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changes of these resonators induced by the electrostatic force via applied dc-bias (pull-in) voltage enable frequency tuning capability of resonators. With the increase of applied dc-bias, the upward frequency shift of resonance caused by boundary condition change offers opposite tuning mechanism to electrical stiffness. As a result, the frequency variation induced by BC-modulation and electrical-stiffness would yield a frequency-insensitive region under a certain dc-bias.

GAP REDUCTION & BC-MODULATION

The motional impedance R_x of a capacitive resonator is determined approximately by the expression

$$R_x = \frac{k_r \cdot d_o^4}{\omega_o Q V_P^2 \varepsilon_o^2 A^2} \quad (1)$$

where k_r, d_o, ω_o, Q, and A are lumped stiffness, electrode-to-resonator gap spacing, radian resonance frequency, quality factor, and overlap area, respectively, of the resonator, and where V_P and ε_o are applied dc-bias and permittivity, respectively. From (1), the most dominant factor to lower motional impedance of a resonator is to reduce its gap spacing d_o of which R_x is proportional to the 4th power. To achieve gap reduction for CMOS-MEMS resonators in Fig. 1(a), soft springs of meander-type supports were designed to provide an easy pull-in scheme for resonators to land on the pull-in stoppers, hence greatly reducing d_o which is determined by the altitude difference between electrode and pull-in stopper as shown in Fig. 1(b). With clever use of the existing CMOS layers (standard TSMC 0.35μm 2P4M CMOS process), three various gap configurations depicted in Fig. 1(b) can be attained by applying dc-bias voltages greater than pull-in threshold. After device pull-in, these three gap configurations of 58nm, 217nm, and 275nm, are achieved by the altitude difference between pull-in stopper and underneath electrode, approximating to thickness difference between Poly-1 and Poly-2 layers (i.e., 58nm), thickness of Poly-2 layer (i.e., 217nm), and thickness of Poly-1 layer (i.e., 275nm), respectively, as shown in Fig. 1(b).

To enhance resonator performance, the beam-array design [8] was utilized to attain lower motional impedance, smaller pull-in voltage, and higher power handling capability than a stand alone resonator. The equivalent motional impedance of an array resonator is given by

$$R_{x\_ARRAY} = \frac{R_x}{n} \quad (2)$$

where n is the number of constituent resonators of the array and R_x is the motional impedance of a stand-alone resonator. In this work, a beam array resonator of Fig. 1(a) with n = 5 was designed utilizing high velocity coupling scheme where the mechanical coupling locations are at the center position (i.e., highest velocity at vibration) of a beam, effectively suppressing the spurious modes in contrast to [8].

To operate this device, the beam-array structure is under pull-in by a dc-bias voltage V_P, hence creating deep-submicron gaps between resonators and their underneath electrodes. Together with the existing dc-bias V_P, an applied ac signal v_i in the input electrode generates an electrostatic force acting vertically on the beam. Then the resulting force drives the resonator into the corresponding vibration mode shape shown in Fig. 2. This motion creates a dc-biased (by V_P) time-varying capacitance that then sources out an output current i_o proportional to the amplitude of vibration. With the increase of applied bias V_P, the mechanical boundary conditions of the vibrating beam array resonator would be gradually transformed from simply-supported BC of Fig. 2(a) (i.e., lower bound frequency) to quasi clamped BC of Fig. 2(b) (i.e., upper bound frequency), leading to an upward frequency shift. To certain level of V_P, the resonance frequency change would be dominated by electrical stiffness with a downward tendency which was observed in experimental results.

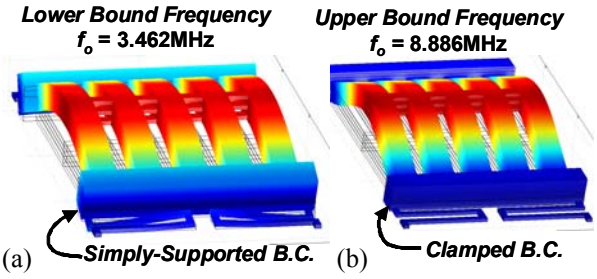


Fig. 2: Finite-element-simulated mode shapes for a CMOS-MEMS beam-array resonator, addressing (a) lower bound and (b) upper bound frequencies of resonance under pull-in.

FABRICATION

A generalized CMOS-MEMS platform [7] using

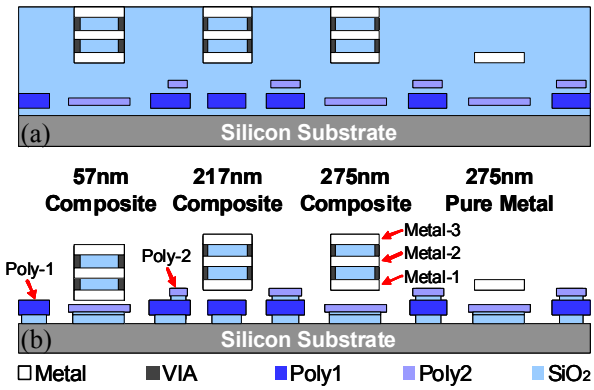


Fig. 3: Cross-sections depicting the fabrication process used to achieve CMOS-MEMS beam-array resonators in this work. (a) After standard CMOS process. (b) After wet release process and pull-in application. Various gap-reduction mechanisms and different structural material configurations are realized in this work.

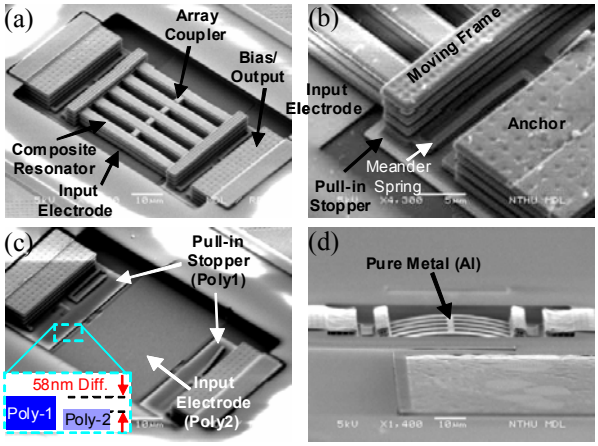


Fig. 4: (a) Full view, (b) zoom-in view, and (c) resonator-removal view of scanning electron micrographs (SEM's) of a fabricated CMOS-MEMS composite beam-array resonator with the 58nm-gap configuration. (d) An SEM of pure-metal beam-array resonator showing serious warping due to residual stress.

0.35μm 2-Poly-4-Metal CMOS service from TSMC was adopted for device fabrication with a cross-section view shown in Fig. 3(a). After post-CMOS release process using commercial SiO_2 wet etchant, sacrificial oxide is removed, leaving (i) composite resonator structures composed of metal and enclosed oxide surrounded by via structure, and (ii) pure-metal resonator structure consisting of Metal-1 (i.e., aluminum) originally used of CMOS interconnects as shown in the right side of Fig. 3(b). Fig. 4 presents SEM's of fabricated beam-array resonators used to evaluate the approach of gap reduction and the scheme of BC-modulated frequency tuning. In Fig. 4(b), soft mechanical springs formed by slender meander-type beams (Metal-1) were designed to lower the pull-in voltage of beam-array structure. The gap reduction scheme can be clearly seen in Fig. 4(c) with the altitude difference of 58nm between the pull-in stopper and underneath electrode.

Issues of residual stress in standard CMOS foundry process usually generate warping on MEMS devices after structure release and Fig. 4(d) shows such phenomenon on a fabricated beam-array resonator using Metal-1 as its structural material right after the wet release process. To investigate the residual stresses of the fabricated beam-array resonators, Fig. 5(a) presents the radius of curvature of 3mm for composite structural materials of Fig. 4(a) while Fig. 5(b) shows 0.18-mm radius of curvature for pure-metal structural material of Fig. 4(d) by using WYKO NT100 optical profiler. The significant warping of pure-metal beam-array resonators hinder the pull-in scheme for gap reduction and make resonance measurement very difficult. Fortunately, the stress issue on the CMOS-MEMS composite beam-array resonator of Fig. 4(a) is greatly relieved using stacked structure shown in Fig. 1(a).

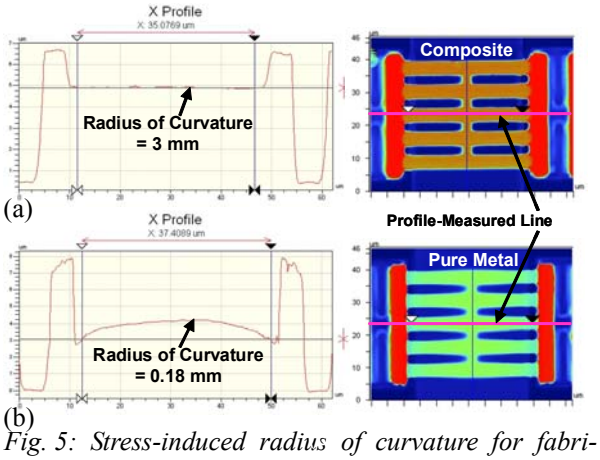


Fig. 5: Stress-induced radius of curvature for fabricated CMOS-MEMS beam-array resonators with (a) composite structural materials and (b) pure-metal structural material after post-CMOS release process.

EXPERIMENTAL RESULTS

The pull-in behavior of a CMOS-MEMS composite beam-array resonator with 58nm-gap-reduction configuration of Fig. 1(a) was measured in Fig. 6 by optical profiler, showing 350nm moving displacement when pull-in occurred at a dc-bias of 32V. Fig. 7 presents the measured spectra for beam-array resonators in three different gap configurations of Fig. 1(b), verifying the motional impedance is greatly improved by the gap reduction schemes with R_x of 87kΩ, 262kΩ, and 524kΩ, respectively, at dc-bias of 110V. Fig. 8 presents the frequency variation versus dc-bias voltage in the 58nm-configuration of Fig. 1(b), showing the resonance frequency tends to increase with bias increased until the saturation occurs at bias around 80V. After saturation of frequency variation, the frequency tendency becomes downward with con-

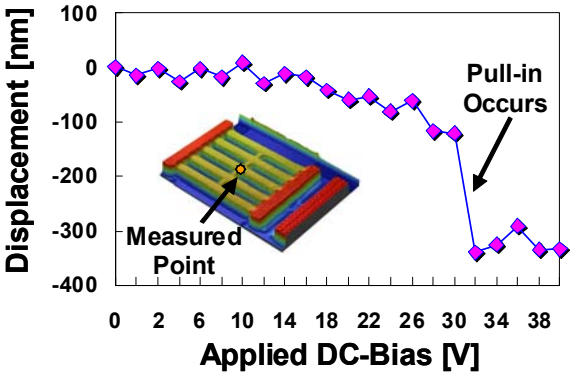


Fig. 6: Displacement of center-measured point versus applied dc-bias for a CMOS-MEMS composite beam-array resonator in its 58nm configuration of Fig. 1(b), indicating pull-in occurred at 32V.

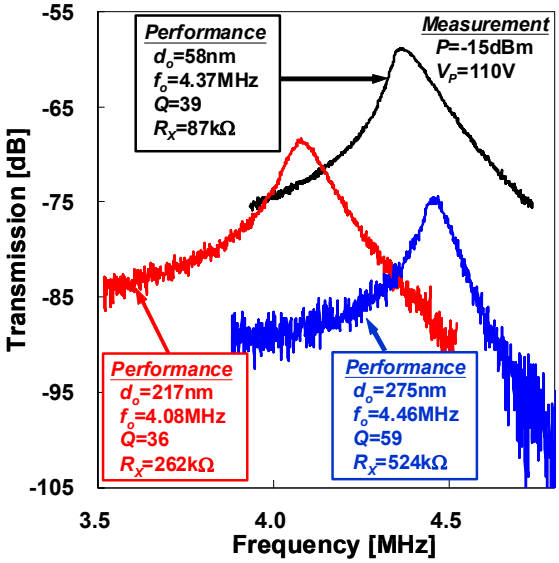


Fig. 7: Measured frequency characteristics of fabricated beam-array resonators for various gap configurations in Fig. 1(b).

tinuous increase of dc bias. Fig. 9 clearly indicates the variation of resonance frequency of composite beam-array resonators is dominated by BC-modulation below dc bias of 80V and dictated by electrical stiffness instead above 80V, hence showing a dc-bias insensitive region of frequency at 80V as a result of the balance between modulated BC and electrical stiffness. Due to constrained boundary conditions in this work, the *Q's* of these composite beam-array resonators were two orders of magnitude lower than conventional micromechanical resonators, therefore hindering further improvement of motional impedance. With *Q's* of 4,000 as an example, motional impedance lower than 1kΩ is plausible by using the gap reduction mechanism of this work.

CONCLUSIONS

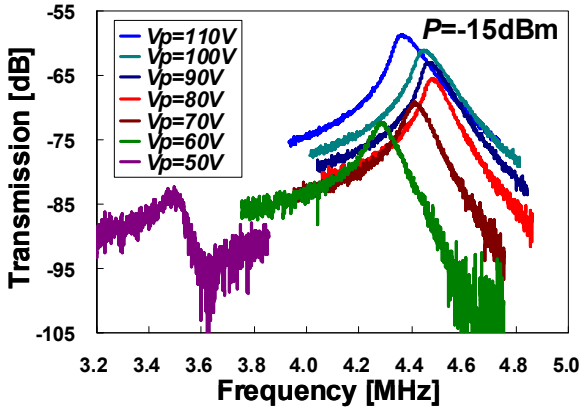


Fig. 8: Measured frequency spectra for a fabricated beam-array resonator with 58nm gap spacing under different bias voltages.

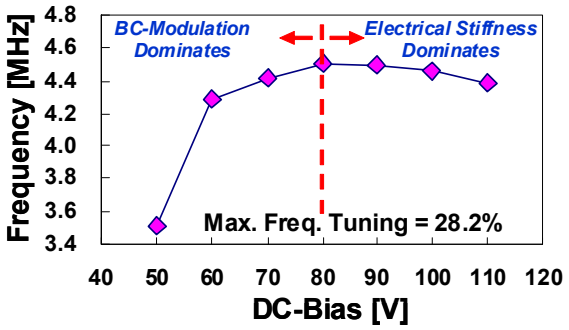


Fig. 9: Frequency variation versus dc-bias, showing two different mechanisms dominate frequency tuning.

An effective approach to achieve sub-micron gap spacing of capacitively-transduced micromechanical resonators fabricated by conventional CMOS foundry process has been demonstrated to greatly lower motional impedance of resonators without the need of costly, advanced CMOS technology. With clever use of the existing CMOS layers, electrode-to-resonator gaps of 58nm, 217nm, and 275nm in CMOS-MEMS resonators have been realized using pull-in scheme of this work, achieving comparable electromechanical coupling compared to non-CMOS-MEMS counterparts. In addition to gap reduction, the resonance frequency of CMOS-MEMS resonators was manipulated by bias-dependent BC-modulation and electrical stiffness, both of which show opposite frequency tuning capability, yielding an insensitive region of frequency under certain dc bias voltage.

ACKNOWLEDGMENT

This work was supported by the National Science Council of Taiwan under grant of NSC-97-2218-E-007-014. The authors also appreciate the TSMC and National Chip Implementation Center (CIC), Taiwan, for supporting the IC Manufacturing.

REFERENCES

[1] C. T.-C. Nguyen, *Trans. Ultrason., Ferroelect., Freq. Contr.*, vol. 54, pp. 251-270, 2007.
[2] G. Piazza, *et al.*, *J. Microelectromech. Syst.*, vol. 16, no. 2, pp. 319-328, 2007.
[3] A. E. Franke, *et al.*, *J. Microelectromech. Syst.*, vol. 12, pp. 160-171, 2003.
[4] K. E. Wojciechowski, *et al.*, *Transducers'09*, Denver, Colorado, USA, pp. 2126-2130, 2009
[5] F. Chen, *et al.*, *MEMS'05*, Miami, Florida, USA.
[6] J. L. Lopez, *et al.*, *J. Micromech. Microeng.*, vol. 19, pp. 1-10, 2009.
[7] W.-C. Chen, *et al.*, *MEMS'10*, Hong Kong, China.
[8] S. Lee, *et al.*, *IEEE Int. Frequency Control Symp.*, Montreal, Canada, pp. 280-286, 2004.

國立清華大學補助員生出國參加國際學術會議報告

序號：

姓　　名	李昇憲	單　　位	奈微所	職　　稱	助理教授
會議期間	Feb. 18-22, 2010		會議地點	Berkeley, CA, USA	
會議名稱	2010 IEEE International Frequency Control Symposium Technical Program Committee Meeting (IFCS'10 TPC Meeting) (2010 IEEE 國際頻率控制研討會技術委員會會議)				
論文名稱	參加 2nd Technical Program Committee Meeting for 2010 IEEE International Frequency Control Symposium, Berkeley, CA, USA				
報告內容	1. IEEE 國際頻率控制研討會已經有五十年以上的歷史，今年六月將於美國 Newport Beach 舉行會議，目前論文投遞已截稿，此次技術委員會(TPC)在技術委員主席 Professor Clark T.-C. Nguyen 的召集下在 Berkeley 舉行，主要任務為決定論文的錄取與否、口頭報告或海報形式、學生論文比賽決選名單、票選 RABI Award、SAWYER Award、CADY Award 等得主，此次共有來自世界各地 213 篇投稿論文；由於此類 TPC 會議是打入國際研究社群非常重要的關鍵，更有助於新進研究人員(如申請人)拓展國際人脈與加強國際研究合作的能量，申請人非常榮幸能夠獲得此一難得之機會，並從中學習如何審查論文、如何順利執行國際會議等，同時申請人也被指定為研討會中 Resonator I Session 的會議主席。 2. 在申請人擔任 TPC 之 Group 1: Materials, Resonators, & Resonator Circuits，共錄取 4 篇邀請論文、28 篇口頭報告論文與 24 篇海報報告論文，本組 TPC				

成員並於會後留下合影，如下圖所示，左起為申請人、Prof. Gianluca Piazza (賓州大學電機系)、Prof. Sunil Bhave (康乃爾大學電機系)、Dr. Yoonkee Kim (U.S. Army Research Laboratory)等；由於今年的重點在於”Miniaturization”，因此吸引許多微機電領域的專家學者投稿，申請人與學生的論文”High-*Q* Integrated CMOS-MEMS Resonators with Deep-Submicron Gaps”亦獲選為口頭報告論文。

本次技術委員會會議圓滿達成任務，也讓我們這些新進委員得以認識其他資深委員，並從深入交流中獲取寶貴的經驗，此會議亦決定六月大會的所有流程，共有 24 個 Parallel Oral Sessions 與 2 個大型 Poster Sessions、工業界展示、辯論會與晚宴等。

3. 本人除了參加技術委員會會議外，亦同時拜訪 Prof. Nguyen 在加州大學柏克萊分校的微機械共振器實驗室，並與其博士班學生進行研究上的討論。

	4. 申請人在這次會議中學習到許多舉辦國際研討會的知識，若未來有機會，相信這次的經驗可以作為將來舉辦大型國際會議的基礎。 5. 在此特別感謝本校提供交通費與生活費的補助，讓申請人能夠順利參與本次技術委員會會議。
附註	報告內容應包括下列各項： 1.參加會議經過 2.與會心得 3.考察參觀活動(無是項活動者省略) 4.建議 5.攜回資料名稱及內容 6.其他

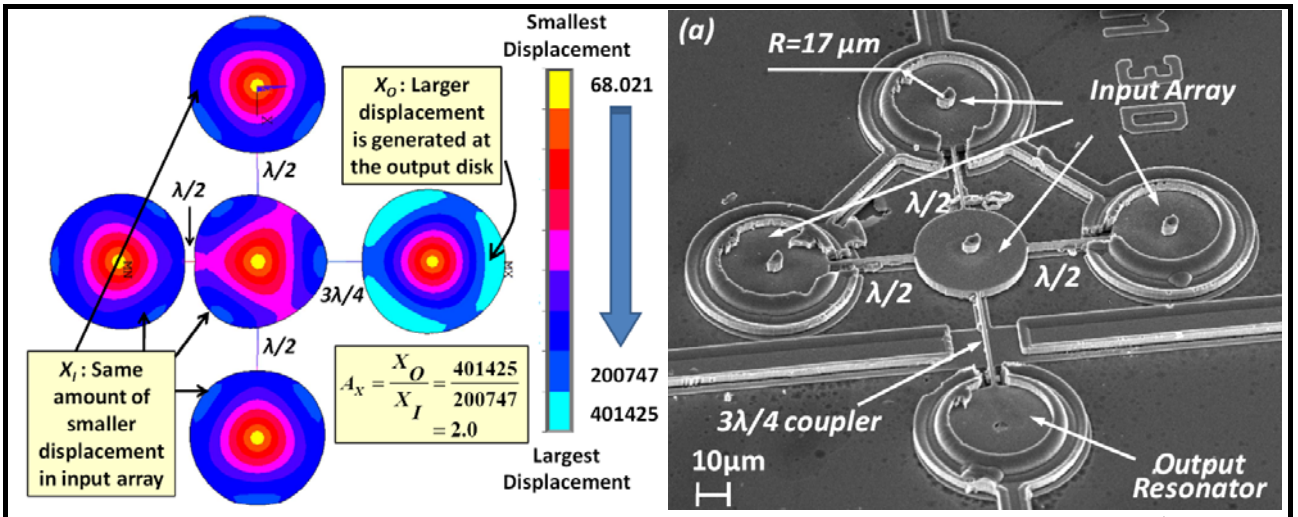
請於回國後一個月內將此表填妥 mail 至 scchung@mx.nthu.edu.tw 信箱

拔尖/增能/一般/新進教師補助計畫**出國報告**

報告繳交日期： 98 年 07 月 29 日

計畫類型	□拔尖計畫 ■增能計畫 □一般計畫 □新進教師補助計畫				
計畫編號	98N2913E1	計畫名稱	應用於無線整合式微系統之奈微機械電路		
出差人	李昇憲	單位系所	奈微所	職稱	助理教授
起迄日期	(98.06.21~98.06.25)		出國地點	USA: Denver, Colorado	
出國目的	參加 2009 第 15 屆國際固態感測器、致動器與微系統學術研討會				
參加會議名稱(若有)	(中文) 2009 第 15 屆國際固態感測器、致動器與微系統學術研討會 (英文) The 15th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers'09)				
發表論文題目(若有)	(中文)數位定義式微機械位移放大器 (英文) DIGITALLY-SPECIFIED MICROMECHANICAL DISPLACEMENT AMPLIFIERS				
經費核銷	拔尖/增能/一般/新進教師補助計畫				17,210 元
	其他計畫經費分攤(奈微所—計畫編號：)				50,000 元

1. 兩年一度的微機電領域盛事—國際固態感測器、致動器與微系統學術研討會(Solid-State Sensors, Actuators and Microsystems, Transducers'09),今年在美國滑雪聖地丹佛 (Denver)舉行。此會議乃是微機電系統(MEMS)領域中規模最大最重要的會議之一。為期五天的時間中，總共有 40 個演講主題，總共 220 場演講發表(oral presentation)，以及 380 篇的海報發表(poster presentation)，投稿篇數超過 1300 篇，總計有 600 篇獲選刊出，刊出論文皆是微機電領域最新之結果。此會議共計超過千名全世界的知名學者參與，其中大會主席為筆者在密西根博士班時期的授課教師與博士論文口試委員 Prof. Khalil Najafi，會中更邀請許多國際知名的學者專家前來演講，Plenary Session 三場演講的首場講者更是密西根大學無線整合微系統研究中心(Center for Wireless Integrated Microsystems)的大家長 Prof. Kensall D. Wise，講授無線整合型微系統在未來健康照護上的應用，由於筆者在密西根大學時期即為此研究中心的一員，從事無線收發器的研究，因此也見證了此一領域的發展；筆者這次亦見到許多過去在密西根大學熟識的師長、無塵室 Staff 與其他實驗室的研究夥伴，內心倍感親切，也交流了未來有可能合作的議題。



2. 筆者與過去實驗室成員共同發表的論文在與會的論文評比中名列前茅，主要探討如何利用設計的方式，在不更改任何製程步驟的條件下，將微機械共振器的位移量放大數倍，運作原理與元件 SEM 如上圖所示；這樣的方式經由模擬與實驗的相互驗證，可望在微機械電路中的功率放大功能扮演非常重要的角色，對於射頻微機電領域的貢獻頗大。
3. 筆者除了參加論文的發表外，亦積極參與本屆研討會各領域專家們的論文發表，尤其在共振器能量損耗機制、Q 值提升與實體間隙換能機制的技術與研究成果上，獲益良多；其他時間並與各領域專家學者廣泛交換研究成果，希望未來能夠將現有技術拓展到其他應用領域。
4. 筆者在這次研討會中，學習到許多舉辦國際研討會的知識，亦經由與知名專家學者的交流，瞭解未來跨領域學門的發展無可限量；若未來有機會，相信這次的經驗可以作為將來舉辦大型國際會議的基礎。
5. 共攜回大會議程手冊與研討會 Proceedings 等相關資料。

在此特別感謝本校提供交通費與生活費的補助，才讓筆者能夠順利參與此次會議。

備註：凡編列國外差旅費的計畫，於返國 15 日內，請填寫本表，以電子郵件傳送至研發處 (cjchang@mx.nthu.edu.tw)，並將核銷單據送至研發處核章。